

100V N-Channel Enhancement Mode Power MOSFET

Description

WMB099N10LG2 uses Wayon's 2nd generation power trench MOSFET technology that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance. This device is well suited for high efficiency fast switching applications

Features

- $V_{DS} = 100\text{ V}$, $I_D = 62\text{ A}$ (Silicon Limited)
 $R_{DS(on)} < 9.9\text{ m}\Omega$ @ $V_{GS} = 10\text{ V}$
 $R_{DS(on)} < 13\text{ m}\Omega$ @ $V_{GS} = 4.5\text{ V}$
- Green Device Available
- Low Gate Charge
- 100% EAS Guaranteed
- High Speed Power Switching, Logic Level

Applications

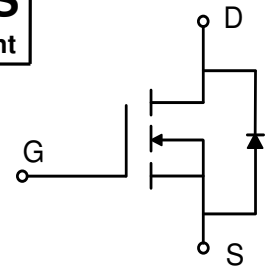
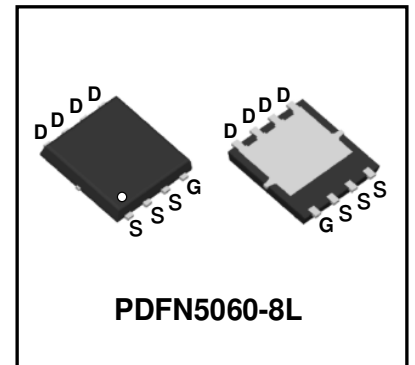
- Hard Switching and High Speed Circuit
- DC/DC Conversion
- Synchronous Rectification in SMPS

Absolute Maximum Ratings

Parameter		Symbol	Value	Unit
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current ¹	$T_C = 25^\circ\text{C}$	I_D	62	A
	$T_C = 100^\circ\text{C}$		40	
Pulsed Drain Current ²		I_{DM}	168	A
Single Pulse Avalanche Energy ³		EAS	80	mJ
Avalanche Current		I_{AS}	40	A
Total Power Dissipation ⁴	$T_C = 25^\circ\text{C}$	P_D	75	W
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal Resistance from Junction-to-Ambient ¹	R_{θJA}	53	$^\circ\text{C/W}$
Thermal Resistance from Junction-to-Case ¹	R_{θJC}	1.6	$^\circ\text{C/W}$



Electrical Characteristics $T_c = 25^\circ\text{C}$, unless otherwise noted

Parameter		Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static Characteristics							
Drain-Source Breakdown Voltage		V _{(BR)DSS}	V _{GS} = 0V, I _D = 250μA	100	-	-	V
Gate-body Leakage Current		I _{GSS}	V _{DS} = 0V, V _{GS} = ±20V	-	-	±100	nA
Zero Gate Voltage Drain Current	T _J =25°C	I _{DSS}	V _{DS} = 100V, V _{GS} = 0V	-	-	1	μA
	T _J =100°C			-	-	100	
Gate-Threshold Voltage		V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250μA	1.4	1.8	2.4	V
Drain-Source on-Resistance ²		R _{DS(on)}	V _{GS} = 10V, I _D = 20A	-	8.2	9.9	mΩ
			V _{GS} = 4.5V, I _D = 20A	-	11.1	13	
Forward Transconductance ²		g _{fs}	V _{DS} = 5V, I _D = 10A	-	78	-	S
Dynamic Characteristics							
Input Capacitance		C _{iss}	V _{DS} = 50V, V _{GS} =0V, f =1MHz	-	1620	-	pF
Output Capacitance		C _{oss}		-	300	-	
Reverse Transfer Capacitance		C _{rss}		-	5.8	-	
Switching Characteristics							
Gate Resistance		R _g	V _{DS} =0V , V _{GS} =0V , f=1MHz	-	1	-	Ω
Total Gate Charge		Q _g	V _{GS} = 4.5V,V _{DS} = 50V, I _D =20A	-	11.6	-	nC
Total Gate Charge		Q _g	V _{GS} = 10V,V _{DS} = 50V, I _D =20A	-	23	-	
Gate-Source Charge		Q _{gs}		-	3.8	-	
Gate-Drain Charge		Q _{gd}		-	6.3	-	
Turn-on Delay Time		t _{d(on)}	V _{GS} =10V, V _{DD} =50V, R _G = 10Ω, I _D = 20A	-	5.9	-	nS
Rise Time		t _r		-	3.9	-	
Turn-off Delay Time		t _{d(off)}		-	17	-	
Fall Time		t _f		-	2.9	-	
Drain-Source Body Diode Characteristics							
Diode Forward Voltage ²		V _{SD}	I _S = 20A, V _{GS} = 0V	-	-	1.2	V
Continuous Source Current ^{1,5}		I _S	V _G =V _D =0V , Force Current	-	-	62	A
Body Diode Reverse Recovery Time		t _{rr}	V _R =50V ,I _F = 20A, di/dt =500A/μs	-	42	-	nS
Body Diode Reverse Recovery Charge		Q _{rr}		-	155	-	nC

Notes:

1. The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
2. The data tested by pulsed, pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
3. The EAS data shows Max. rating. The test condition is $V_{DD}=25V, V_{GS}=10V, L=0.1mH, I_{AS}=40A$
4. The power dissipation is limited by 150°C junction temperature
5. The data is theoretically the same as I_D and I_{DM} , in real applications, should be limited by total power dissipation.

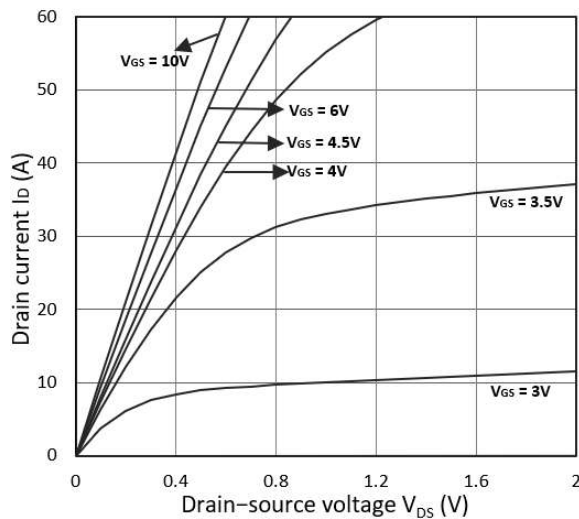


Figure 1. Output Characteristics

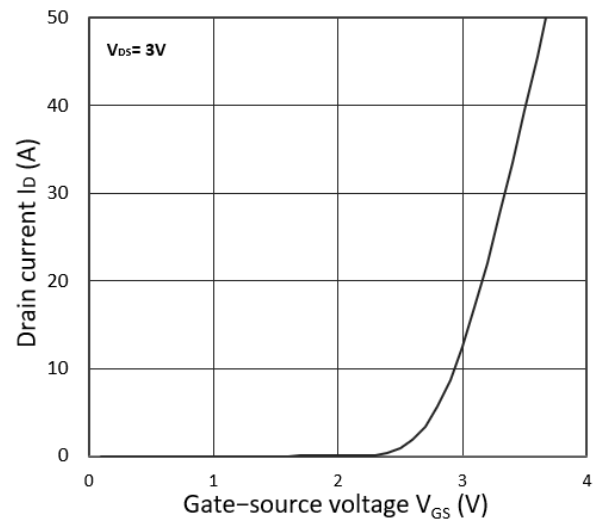


Figure 2. Transfer Characteristics

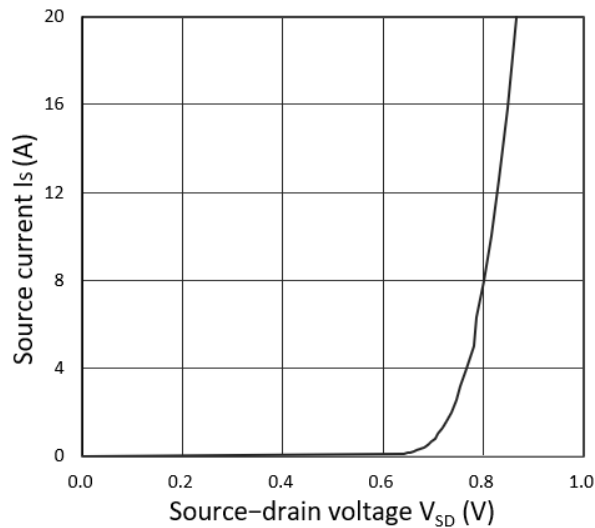


Figure 3. Forward Characteristics of Reverse

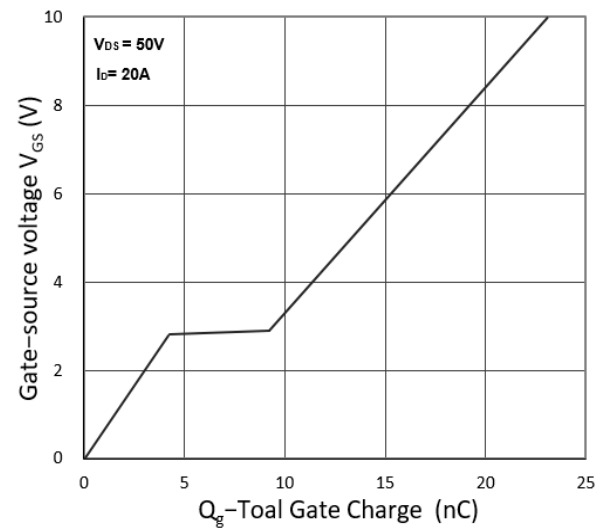
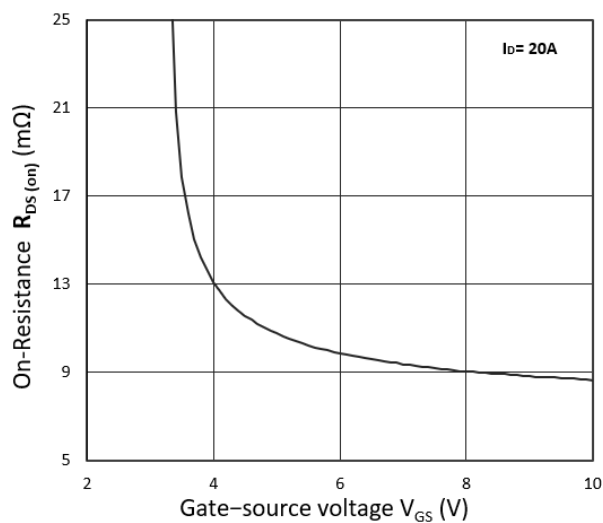
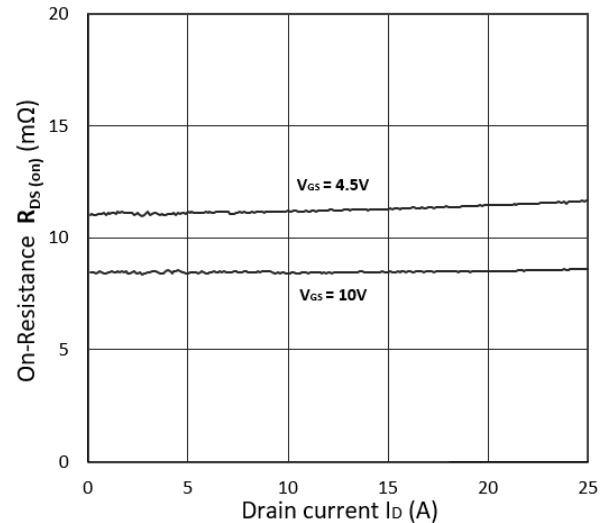


Figure 4. Gate Charge Characteristics

Figure 5. $R_{DS(ON)}$ vs. V_{GS} Figure 6. $R_{DS(ON)}$ vs. I_D

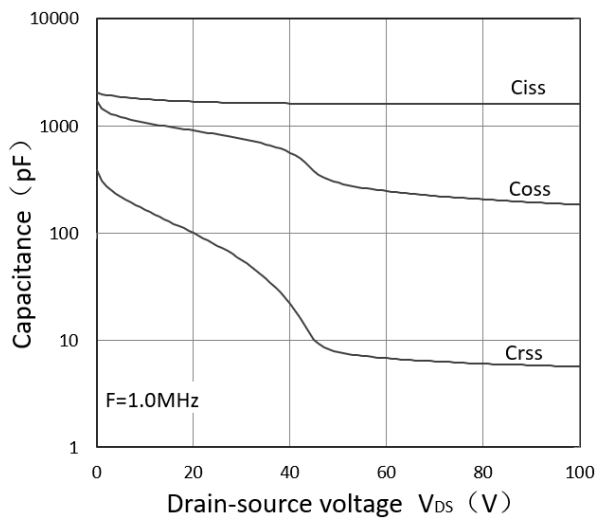


Figure 7. Capacitance Characteristics

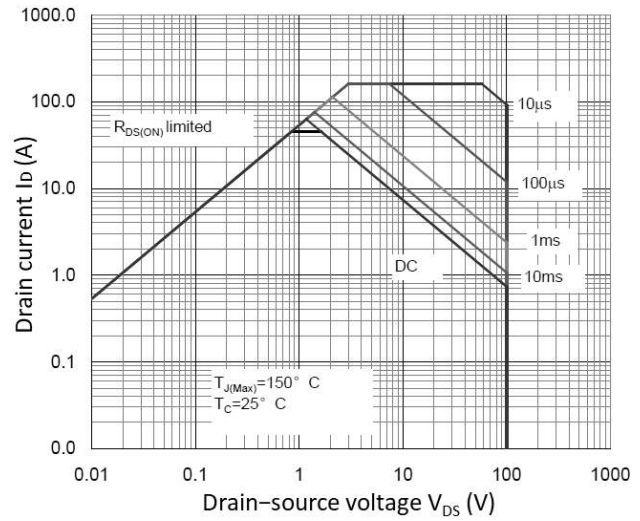


Figure 8. Safe Operating Area

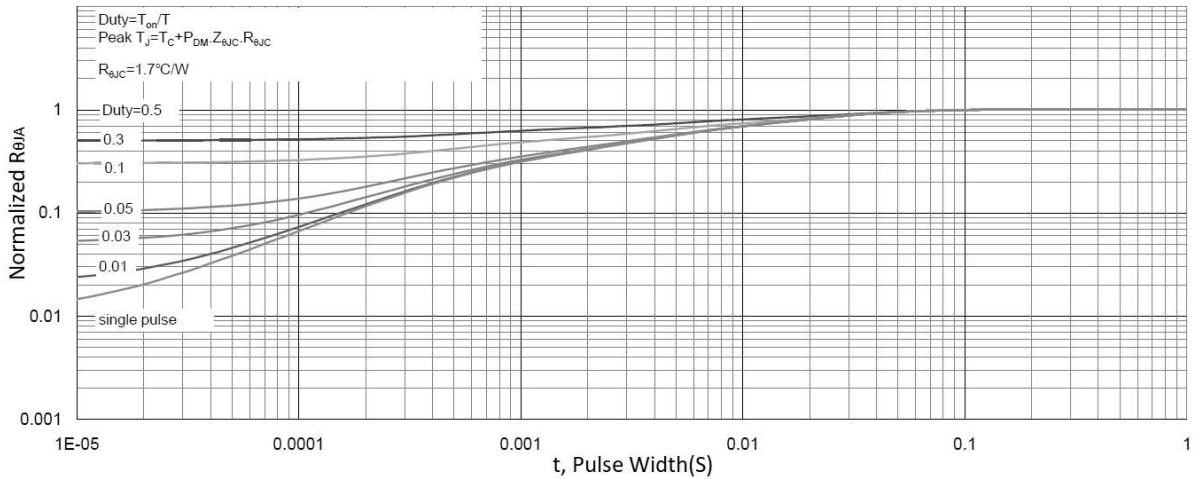


Figure 9. Normalized Maximum Transient Thermal Impedance

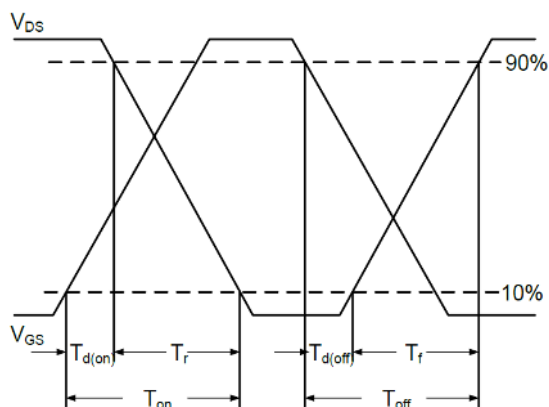
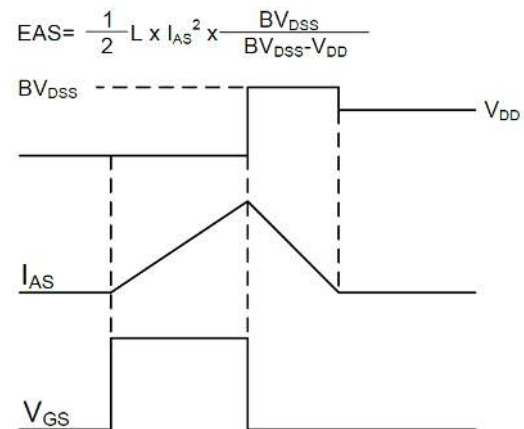
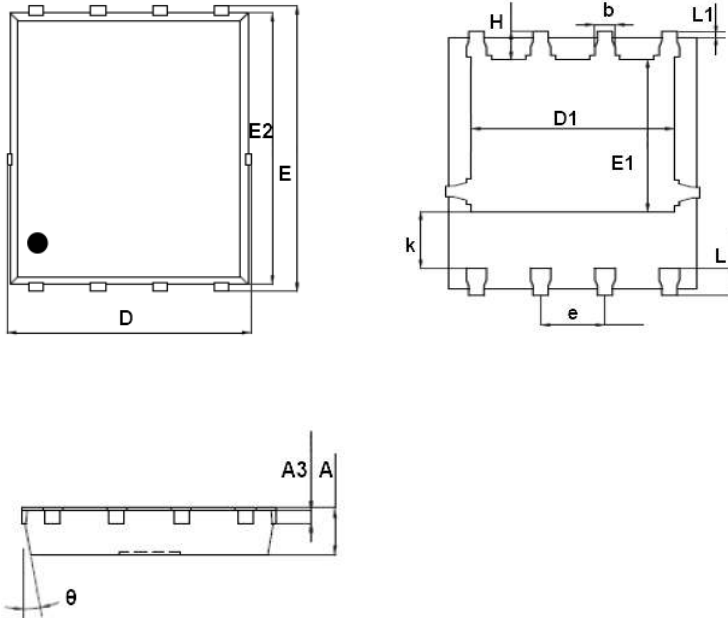


Figure 10. Switching Time Waveform

Figure 11. Unclamped Inductive Switching
Waveform

Mechanical Dimensions for PDFN5060-8L

COMMON DIMENSIONS

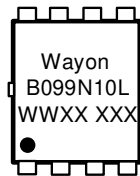


SYMBOL	MM	
	MIN	MAX
A	0.90	1.20
A3	0.15	0.35
D	4.80	5.40
E	5.90	6.35
D1	3.61	4.31
E1	3.30	3.92
E2	5.65	6.06
k	1.10	-
b	0.30	0.51
e	1.27BSC	
L	0.38	0.71
L1	0.05	0.36
H	0.38	0.61
θ	0°	12°

Ordering Information

Part	Package	Marking	Packing method
WMB099N10LG2	PDFN5060-8L	B099N10L	Tape and Reel

Marking Information



B099N10L = Device code

WWXX XXX= Date code

Contact Information

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